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Family of ZVT Interleaved Converters with Low Number of Components

Baharak Akhlaghi, *Student Member, IEEE,* and Hosein Farzanehfard, *Member, IEEE*

***Abstract*—This paper presents a family of ZVT interleaved DC/DC converters. Soft switching operation for all power semiconductor devices in the proposed topologies is achieved by using one auxiliary circuit with only one auxiliary switch. Therefore, the proposed converters have a simple structure with low size and cost. The proposed converters can achieve zero voltage soft switching operation for the main switches and zero current soft switching operation for the auxiliary switch. In addition, the reverse recovery problem of the diodes is alleviated. Therefore, the losses associated with semiconductor components are reduced and efficiency is improved considerably. Besides, no extra voltage and current stresses are imposed on the main switches in comparison with hard switching counterparts. Operation principles and design considerations of an interleaved boost converter with the ZVT auxiliary circuit are discussed in details. A prototype of this converter is implemented and tested to validate the theoretical analysis and converter operation.**

***Index Terms*—Interleaved converters, PWM, soft switching, ZVT.**

I. Introduction

RECENTLY interleaved DC/DC converters are widely employed in many applications such as power factor correction (PFC) converters, voltage regulator (VR) modules, and interface circuits in renewable energy systems [1]–[3]. Reduction of the current ripple, improved transient response, better thermal distribution and reliability are some of the benefits of interleaved converters [4], [5]. In multi-phase interleaved converters, the overall current ripple magnitude is reduced and the effective input current frequency is increased by the number of phases multiplied by the switching frequency of one phase [5], [6]. Furthermore, in the high power multi-phase interleaved converters, current is shared between the phases. Therefore, the power semiconductor devices current stress and also conduction losses are reduced.

High switching frequency can improve the power density and transient response of DC/DC converters [4]. However, at high frequencies, the switching losses increase and result in lower efficiency [7], [8]. Moreover, in high frequency hard-switched converters, the electromagnetic interferences (EMI) cause severe problems [8]. Soft switching passive [9], [10] or active [7], [8] techniques can eliminate switching losses and diminish the EMI problems. Zero voltage transition (ZVT) [11]–[13] is an active soft switching technique preferred for the converters in which MOSFET is used as an active switch. This technique can remove MOSFET switching and capacitive turn on losses. In ZVT interleaved converters, reducing the number of elements in the ZVT cell and also using a single cell for multi-phase interleaved converters can significantly decrease the size and cost. Recently, some studies are published in the field of ZVT interleaved boost [14]–[23], buck [24] and [25], and buck-boost [26] converters. However, the introduced converters have at least one of the following key drawbacks.

1) Large number of passive or active auxiliary elements which increases the circuit complexity, size, and cost.
2) The auxiliary switch or diodes are hard-switched which contributes to switching losses and EMI.
3) One or more switches need floating gate driver which adds to complexity of control circuit.

A fully soft-switched ZVT interleaved boost converter is introduced in [14]. Its auxiliary circuit in a two-phase interleaved boost converter requires two auxiliary switches. Furthermore, the main switches current stress is high. In [15], a fully soft-switched multi-phase interleaved boost converter with a ZVT cell using a single resonant inductor is proposed. However, it uses one unidirectional auxiliary switch with floating gate driver for each phase. In order to reduce the number of active auxiliary switches, some other topologies are recently introduced [16]–[23]. Interleaved boost converters of [16]–[18] can provide soft switching operation for the main switches by using a single auxiliary switch. However, in these structures, the auxiliary semiconductor devices are hard-switched. In [16], the auxiliary switch is triggered four times in each switching cycle which further exacerbates the situation. In [17], the auxiliary switch must be turned on for a long time and all the power stored in the auxiliary circuit is dissipated in the converter. A fully soft-switched interleaved boost converter with no extra current and voltage stresses on the main switches is presented in [19]. This converter needs numerous auxiliary elements including four diodes and two extra auxiliary inductors in a two-phase interleaved structure. A ZVT interleaved boost converter with one auxiliary switch

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Baharak Akhlaghi and Hosein Farzanehfard are with the Department of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan 84156-83111, Iran (e-mail: baharak.akhlaghi@ec.iut.ac.ir; hosein@cc.iut.ac.ir).

(corresponding author to provide e-mail: hosein@cc.iut.ac.ir).

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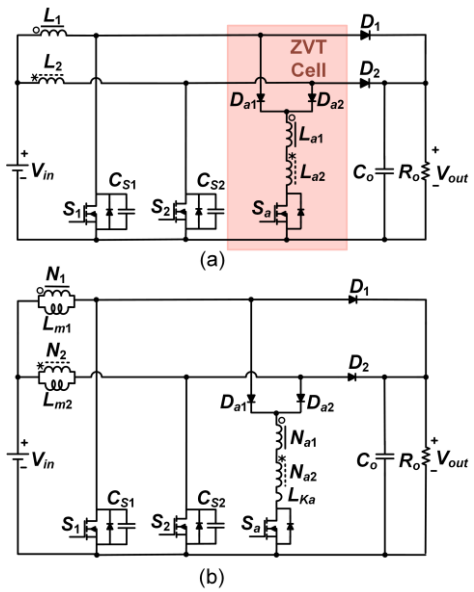

Fig. 1. (a) Proposed ZVT interleaved boost converter. (b) Equivalent circuit.

is introduced in [20]. This converter is fully soft-switched, but the bulky auxiliary circuit requires an extra transformer with high peak current which delivers energy to the load in the entire on-time transition of the auxiliary switch. This leads to increase of conduction losses. Interleaved soft switching converters with low number of components are presented in [21]–[23]. However, the converter introduced in [21] is frequency controlled and thus, its filter design is not optimum. Besides, extra current stress is imposed on the converter switches. The converter of [22] requires a separate core for its auxiliary inductor and floating gate driver circuit for its auxiliary switch. In the converter introduced in [23], although the ZVT topology does not utilize any auxiliary switch, but the role of the auxiliary switches is played by its synchronous rectifier switches. Hence, this soft switching cell is only applicable to the converters with synchronous rectifiers. Besides, extra current stress on switches and circulating losses exist in this converter.

A fully soft switched ZVT interleaved buck converter is proposed in [24] which utilizes an auxiliary circuit with only one active switch. However, it has numerous auxiliary components and the voltage and current stresses of the auxiliary switch is high. An interleaved twin-buck converter with low number of auxiliary elements is presented in [25], nevertheless, such as the topology introduced in [21], it is frequency controlled.

Similar to the structure of the converter proposed in [21] and [25], an interleaved buck-boost converter is introduced in [26]. Although its number of the auxiliary elements is low, it suffers from the same drawbacks as [21] and [25].

This paper presents a family of ZVT interleaved converters and its variants in which all of the semiconductor devices operate under fully soft switching condition by using only one auxiliary circuit with a single switch and no extra inductor to improve the efficiency in a wide range of load variations. In the proposed converters, zero voltage switching (ZVS) operation for the main switches and zero current switching (ZCS) operation for the auxiliary switch is achieved. Besides, the leakage inductance of applied coupled inductors can control the current falling rate of the output and the auxiliary diodes which alleviates the reverse recovery problem of the diodes. The employed coupled inductors act as voltage dependent voltage sources, forcing the auxiliary circuit current to reduce to zero after accomplishing ZVS operation for the main switch at turn on. These two inductors have used the already existing cores in the converter. The applied ZVT cell absorbs the leakage inductances of these two coupled inductors and also utilizes the MOSFET parasitic capacitors energy as the required snubber capacitors. Therefore, extra resonant and snubber inductors can be omitted. Hence, the size, weight and cost of the auxiliary circuit are reduced considerably. The theoretical analysis along with the design procedure of the boost type of the proposed ZVT interleaved converters family are provided. A 200 W prototype of the interleaved boost converter operating at 100 kHz is implemented and the experimental results are presented. Other members of the proposed ZVT interleaved converters family are presented. Furthermore, in order to make the proposed ZVT interleaved converters more compact and establish automatic current sharing in the interleaved modules, variants of the ZVT interleaved converters family are introduced. The basic ZVT cell is introduced in [27], but its implementation is limited to single-phase converters and did not address any other types of DC/DC interleaved converters. In this paper, the cell is developed and applied to create a fully soft-switched, compact and low cost family of ZVT interleaved converters with only one common auxiliary circuit.

II. Proposed ZVT Interleaved Boost Converter

Fig. 1(a) shows the proposed ZVT interleaved boost converter. The ZVT cell is shown in the block. The primary windings of the coupled inductors, L_1 and L_2, are coupled to the secondary windings in the auxiliary circuit, L_{a1} and L_{a2}, respectively. S_1 and S_2 are the main switches; D_1 and D_2 are the output diodes; V_{in} and V_{out} denote the input and output voltages, respectively; C_{S1} and C_{S2} are the snubber capacitors of S_1 and S_2, respectively; C_o is the output filter capacitor; and R_o is the load. The equivalent circuit of the converter is demonstrated in Fig. 1(b) where N_1 and N_2 are the primary windings number of turns, and N_{a1} and N_{a2} are the secondary windings number of turns in the coupled inductors; L_{m1} and L_{m2} are the magnetizing inductances; L_{Ka} is the equivalent of the secondary leakage inductance and the reflected inductance from the primary to the secondary side; S_a is the auxiliary switch, and D_{a1} and D_{a2} are the auxiliary diodes. It is assumed that N_1=N_2=N and N_{a1}=N_{a2}=N_a. The turns ratio N_a/N is defined by n. Soft switching in the proposed converters is achieved for duty cycle (D) values less and greater than 0.5. The converter operation for D>0.5 is presented as follows.

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There are fourteen operational modes during each switching period. Due to the symmetrical structure of the interleaved topology, only seven modes related to the main switch S_1 are analyzed. Fig. 2 and 3 show the key waveforms and the equivalent circuits of each operational mode, respectively.

Prior to t_0, it is assumed that S_2 and D_1 are in ON state and all other semiconductor devices are OFF. C_{S1} is charged to V_{out}.

Mode 1 [t_0-t_1] (*Fig.* 3(*a*)): In order to discharge C_{S1} and have ZVS turn on for S_1, just before applying S_1 gate signal the auxiliary circuit must be activated. Thus, at t_0, S_a is turned on at ZCS due to the series leakage inductance, L_{Ka}. By turning S_a on, D_{a1} turns on at ZCS as well. Because of positive voltage across L_{Ka}, its current, I_{Lka} starts to increase and conversely, the output diode current, I_{D1} decreases linearly. At t_1, I_{D1} reaches zero and D_1 turns off at ZCS and this mode ends. For this interval, the following equations are valid:

$$I_{L_{ka}}(t) = \frac{V_{out}[1-n(1-2D)]}{L_{Ka}}(t-t_0) \tag{1}$$

$$I_{D_1}(t) = I_{L_{m1}} - (n+1)I_{L_{Ka}}(t) \tag{2}$$

where I_{Lm1} is L_{m1} current and is equal to half of the average input current (I_{in}/2), assuming current sharing between two phases.

Mode 2 [t_1-t_2] (*Fig.* 3(*b*)): At t_1, D_1 turns off and a resonance begins between C_{S1} and L_{Ka}. At the end of this mode, C_{S1} energy is completely delivered to L_{Ka} and C_{S1} voltage, V_{CS1} decreases to zero. Afterward, S_1 and S_2 antiparallel diodes turn on. For this resonance, the following equations can be written:

$$I_{L_{ka}}(t) = A + B\sin(\omega(t-t_1)) \tag{3}$$

$$V_{C_{S1}}(t) = \frac{1}{n+1}\left(L_{Ka}\frac{dI_{L_{Ka}}}{dt} + 2nV_{in}\right) \tag{4}$$

where

$$\omega = \frac{n+1}{\sqrt{L_{K_a}C_{S_1}}} \tag{5}$$

$$A = \frac{I_{L_m}}{n+1} \tag{6}$$

$$B = \frac{V_{out}[1-n(1-2D)]}{\omega L_{Ka}}. \tag{7}$$

Mode 3 [t_2-t_3] (*Fig.* 3(*c*)): At t_2, S_1 and S_2 antiparallel diodes turn on. In this mode, I_{Lka} ramps down due to the voltage dependent voltage source with value of $-(V_{La1}+V_{La2})=-2nV_{in}$ caused by the reflection of the L_1 and L_2 voltages to the secondary side. At t_3, S_1 and S_2 antiparallel diodes turn off at ZCS and this mode ends. During this interval, S_1 gate signal can be applied and this switch can be turned on at ZVS. For this mode the following equation can be written:

$$I_{Sa}(t) = I_{L_{ka}}(t) = I_{L_{ka}}(t_2) - \frac{2n(1-D)V_{out}}{L_{Ka}}(t-t_2) \tag{8}$$

where $I_{Lka}(t_2)$ can be extracted from (3) by substituting t by t_2.

Mode 4 [t_3-t_4] (*Fig.* 3(*d*)): In this mode, I_{Lka} continues to decrease linearly with the same slope until it goes to zero at t_4 and S_a turns off at ZCS.

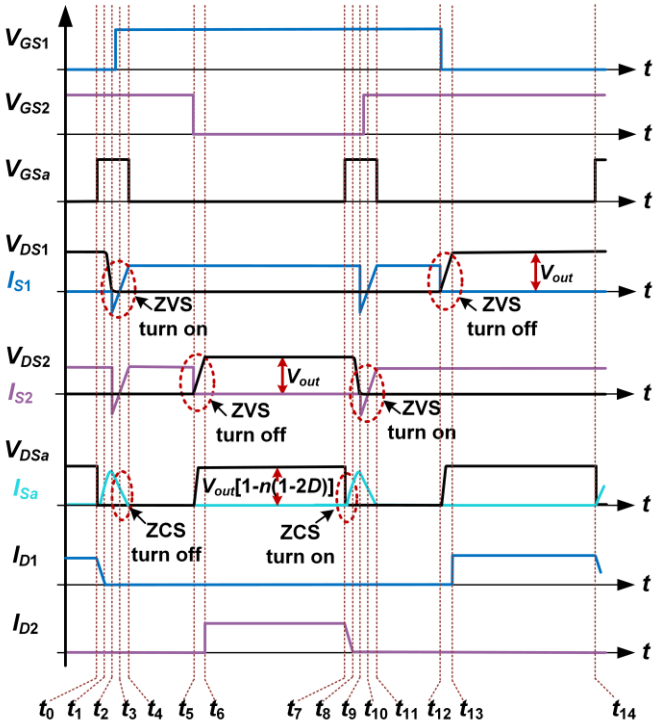

Fig. 2. Key waveforms of the proposed ZVT interleaved boost converter.

Mode 5 [t_4-t_5] (*Fig.* 3(*e*)): During this mode, both main switches are ON and the auxiliary circuit is not active. L_{m1} and L_{m2} are being linearly charged by the input voltage source, V_{in}. The output capacitor is supplying the load.

Mode 6 [t_5-t_6] (*Fig.* 3(*f*)): At the beginning of this mode, S_2 is turned off at ZVS due to its snubber capacitor, C_{S2}. During this transition, L_{m2} current charges C_{S2} almost linearly. At t_6, S_2 drain-source voltage (V_{DS2}=V_{CS2}) has increased to V_{out}, and D_2 turns on. For this interval the following equation can be written:

$$V_{DS_2} = V_{C_{S2}} = \frac{I_{L_{m2}}}{C_{S_2}}(t-t_4) \tag{9}$$

where I_{Lm2} is L_{m2} current.

Mode 7 [t_6-t_7] (*Fig.* 3(*g*)): In this mode, the stored energy of L_{m2} is being transferred to the output. Simultaneously, L_{m1} is being linearly charged by V_{in}. At t_7, the next half a switching cycle begins and the auxiliary switch turns on again to provide ZVS condition for S_2 at turn on.

III. Soft Switching Range and Conditions

In order to provide ZVS condition for the main switch at turn on instant, the output diode D_1 must be turned off at t_1 so that a resonant loop consisting of the auxiliary circuit elements namely L_{Ka}, C_{S1}, and the voltage induced by the coupled inductors can be formed to discharge C_{S1}. Consequently, the voltage induced on the coupled inductors in the auxiliary circuit must be smaller than the output voltage. Considering this fact, the following relation is obtained:

$$V_{out} \geq \frac{2n}{n+1}V_{in}. \tag{10}$$

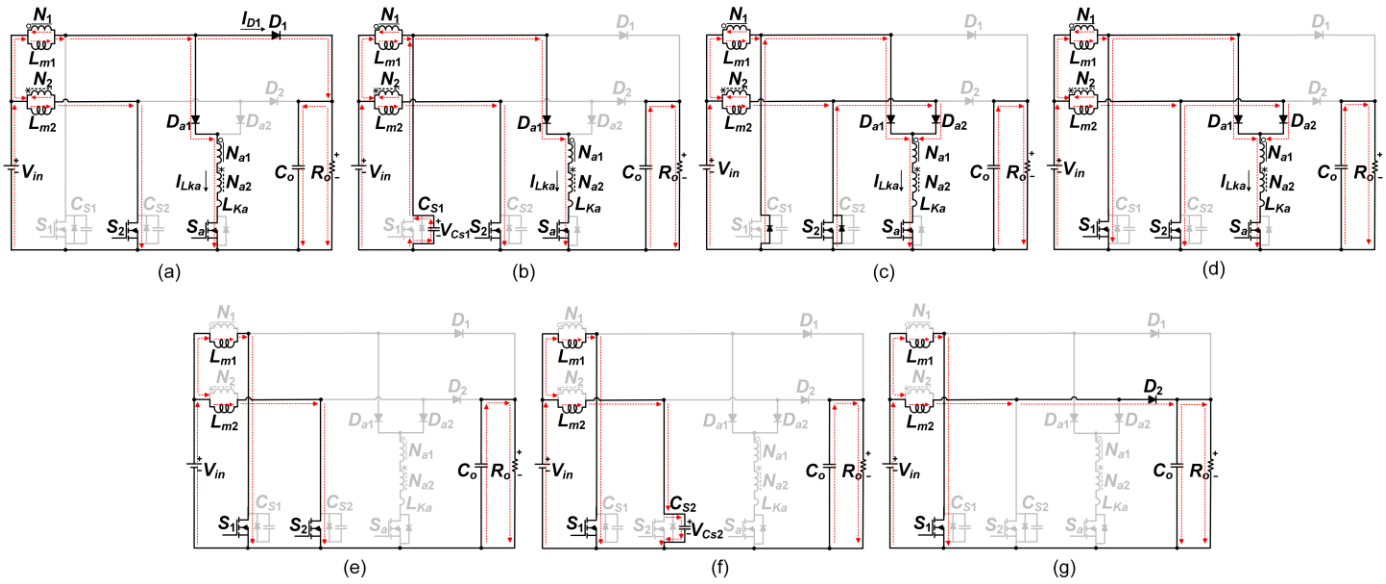

Fig. 3. Equivalent circuits of each operating mode. (a) Mode 1 [t_0-t_1]. (b) Mode 2 [t_1-t_2]. (c) Mode 3 [t_2-t_3]. (d) Mode 4 [t_3-t_4]. (e) Mode 5 [t_4-t_5]. (f) Mode 6 [t_5-t_6]. (f) Mode 7 [t_6-t_7].

This relation holds for any values of n>0. Regarding (4), C_{S1} can be completely discharged in mode 2, if the following requirement is satisfied:

$$\left|\frac{2n(1-D)V_{out}}{B\omega L_{K_a}}\right| \le 1. \tag{11}$$

The minimum required time for the main switch snubber capacitor to be discharged and forward bias its antiparallel diode is defined as t_{ZVT} which is the summation of modes 1 and 2 durations. In other words, t_{ZVT} is the minimum required advanced time before applying the main switch gate signal, and is given by:

$$t_{ZVT} = \frac{I_{L_m} L_{K_a}}{(n+1)[1-n(1-2D)]V_{out}} + \frac{1}{\omega}\cos^{-1}\left(\frac{2n(1-D)V_{out}}{B\omega L_{K_a}}\right). \tag{12}$$

ZVS condition at turn off for the main switches and ZCS condition at turn on for the auxiliary switch are provided by their snubber capacitor and snubber inductor, respectively.

In order to generate ZCS condition for the auxiliary switch at turn off, the auxiliary switch gate signal must be removed when I_{Sa} reaches zero. The total time that the auxiliary switch must be kept ON to provide ZVS condition at turn on for the main switch and then turn off at ZCS condition, t_{ZCT} is the summation of t_{ZVT} and durations of modes 3 and 4, and is given by:

$$t_{ZCT} = t_{ZVT} + \frac{L_{Ka} I_{L_{Ka}}(t_2)}{2n(1-D)V_{out}}. \tag{13}$$

IV. Design Procedure and Example

The design procedure for the proposed converter is explained and the converter parameters are calculated through an example of a two-phase ZVT interleaved boost converter with the input voltage V_{in}=90-110 V, the output voltage V_{out}=400 V, the full load output power P_{out}=200 W, and the switching frequency f_{sw}=100 kHz. Due to the symmetry of the interleaved structure, it is assumed that L_{m1}=L_{m2}=L_m, C_{S1}=C_{S2}=C_S, and S_1 is identical to S_2, so as D_1 to D_2.

A. Selection of Passive Elements

The magnetizing inductances (L_{m1} and L_{m2}) which serve as the boost inductors, and the output capacitor (C_o) are designed like an ordinary boost converter [28]. As shown in Table I, a 47 μF electrolyte capacitor is used for C_o and the value of L_m is 2 mH for CCM operation.

B. Selection of Semiconductor Elements

The maximum voltage and current of the main switches and the output diodes are like those of a conventional boost converter as below:

$$V_{DS_{1,2(\max)}} = V_{D_{1,2(\max)}} = V_{out} \tag{14}$$

$$I_{S_{1,2(\max)}} = I_{D_{1,2(\max)}} = I_{L_{m1,2(\max)}} + \frac{\Delta I_{L_{m1,2}}}{2} \tag{15}$$

where $I_{Lm1,2(\max)}$=$I_{in(\max)}$/2 and $\Delta I_{Lm1,2}$ is chosen to ensure CCM operation of the converter at light load, in this case 25% of nominal output power. $I_{in(\max)}$ is obtained assuming minimum efficiency of 0.9 and using the relation between the input power with respect to the input current.

The maximum voltage and current of the auxiliary switch and diodes are calculated as below:

$$V_{Sa(\max)} = [1-n(1-2D_{\max})]V_{out} \tag{16}$$

$$V_{D_{a1(\max)}} = V_{D_{a2(\max)}} = 2n(1-D_{\min})V_{out} \tag{17}$$

$$I_{S_{a(\max)}} = I_{D_{a1,2(\max)}} = \frac{I_{L_{m1,2(\max)}}}{(n+1)} + \frac{V_{out}[1-n(1-2D_{\max})]}{\omega L_{Ka}}. \tag{18}$$

According to (14) and (15), the voltage stress of the main switches and the output diodes is equal to 400 V and their

TABLE I
THE PROPOSED INTERLEAVED BOOST CONVERTER SPECIFICATION

Parameter	Symbol	Specification
Input voltage	V_{in}	90-110 V
Output voltage	V_{out}	400 V
Output power	P_{out}	200 W
Main and auxiliary switches	S_1, S_2, S_a	IPP50R199CP
Output and auxiliary diodes	D_1, D_2, D_{a1}, D_{a2}	MUR460
Output capacitor	C_o	47 µF
Magnetizing inductance	L_m	2 mH
Leakage inductance	L_{Ka}	5 µH
Snubber capacitors	C_{S1}, C_{S2}	1 nF
Turns ratio	n	0.3

maximum current is equal to 1.43 A and their root mean square (RMS) current at the full load output power is equal to 1.08 A. Therefore, IPP50R199CP and MUR460 can be selected as the main switches and diodes, respectively. As it is explained in the following section, the same switch and diode can be utilized for the ZVT cell semiconductors.

C. Auxiliary Circuit Design

The auxiliary circuit components are mainly designed based on providing soft switching for the switches, and concurrently soft switching condition is established for the rest of semiconductor elements. Due to the simple structure of the auxiliary circuit, only proper values for L_{Ka}, C_S, and n should be selected.

1) The equivalent leakage inductance, L_{Ka} plays two main roles in the auxiliary circuit, as a turn on snubber to control *di/dt* of the auxiliary switch, and as a resonant inductor to discharge the snubber capacitor in mode 2. The minimum values of snubber capacitors and inductor can be obtained as explained in [29] equal to 0.1 nF and 2.63 µH, respectively. Thus, by considering the required overdesign, 5 µH is selected for the snubber inductor for which the leakage inductance can be utilized. This value can be easily extracted from the coupled inductors. However, if the value of the leakage inductance would be different in practical condition, the design procedure should be repeated with the measured value. For C_S, there are other conditions which are presented in the following and must be taken into account.
2) $I_{Lka}(t_2)=I_{Sa(\max)}$ must be greater than summation of $I_{Lm1(\max)}$ and $I_{Lm2(\max)}$ so that S_1 and S_2 antiparallel diodes can be turned on in mode 3 and ZVS turn on condition can be achieved for the main switch. $I_{Lm1,2(\max)}$ is obtained as 1.43 A. Considering proper overdesign, $I_{Lka(\max)}$ should be greater than 4 A.
3) After that L_{Ka} discharges the snubber capacitor, the auxiliary switch must be turned off at the earliest possible time to reduce the conduction losses of the auxiliary circuit and impose less limitations on *D*. Besides, it should be turned off before the main switch S_2 turns off. In other words, the duration of modes 3 and 4 ($t_{24}=t_4-t_2$) must be much smaller $t_{25}=t_5-t_2$ in Fig. 2:

$$t_{25_{(\min)}} = D_{\min} T_{sw} - \frac{T_{sw}}{2} \tag{19}$$

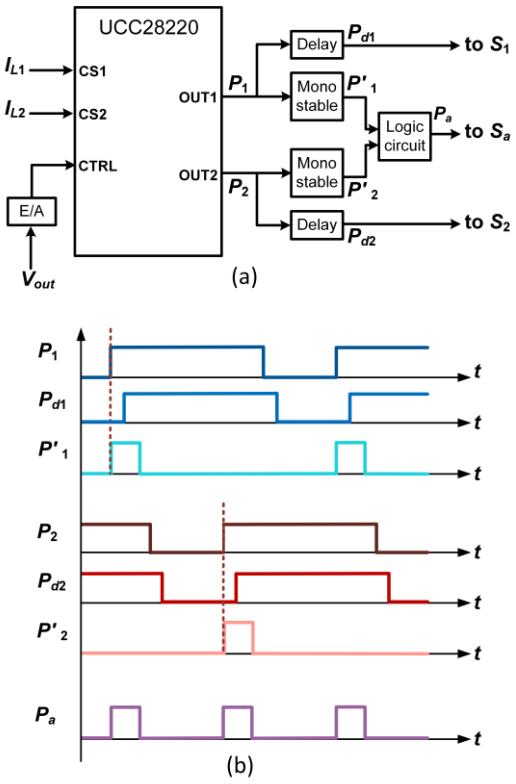

Fig. 4. (a) Block diagram of control unit. (b) Generated pulses.

$$t_{24_{(\max)}} \le 0.2 \times t_{25_{(\min)}} \tag{20}$$

where T_{sw} is the switching period. Thus, considering (8), n should be greater than 0.25 to satisfy (20).

4) The fourth condition is about the auxiliary switch voltage stress which is considered to be lower than 1.2 times the main switch voltage stress. Thus, from (16) n should be less than 0.36. Considering the conditions 3 and 4, n is selected as 0.3.
5) The resonance period in mode 2 is selected less than 10 % of the switching period. From (6), C_S should be less than 8.6 nF.
6) The auxiliary switch current stress should be less than $2\times(I_{Lm1(\max)}+I_{Lm2(\max)})$. Therefore, from (18), C_S should be less than 1.5 nF.

Therefore, from the conditions 1, 5, and 6, C_S value is selected equal to 1 nF.

By choosing these values for L_{Ka}, C_S, and n, conditions set by (10) and (11) are always satisfied. The voltage stresses of the auxiliary switch and diode are respectively about 470 V and 70 V. Their RMS current is equal to 1.24 A.

V. EXPERIMENTAL RESULTS

In order to confirm the analytical analysis, a prototype of the ZVT interleaved boost converter is implemented and tested in the laboratory. The important elements and parameters used are listed in Table I.

As shown in the control block diagram of Fig. 4(a), a current mode control IC (UCC28220 from Texas Instruments) is utilized for the proposed converter to ensure equal current sharing between interleaved modules. In addition, monostable

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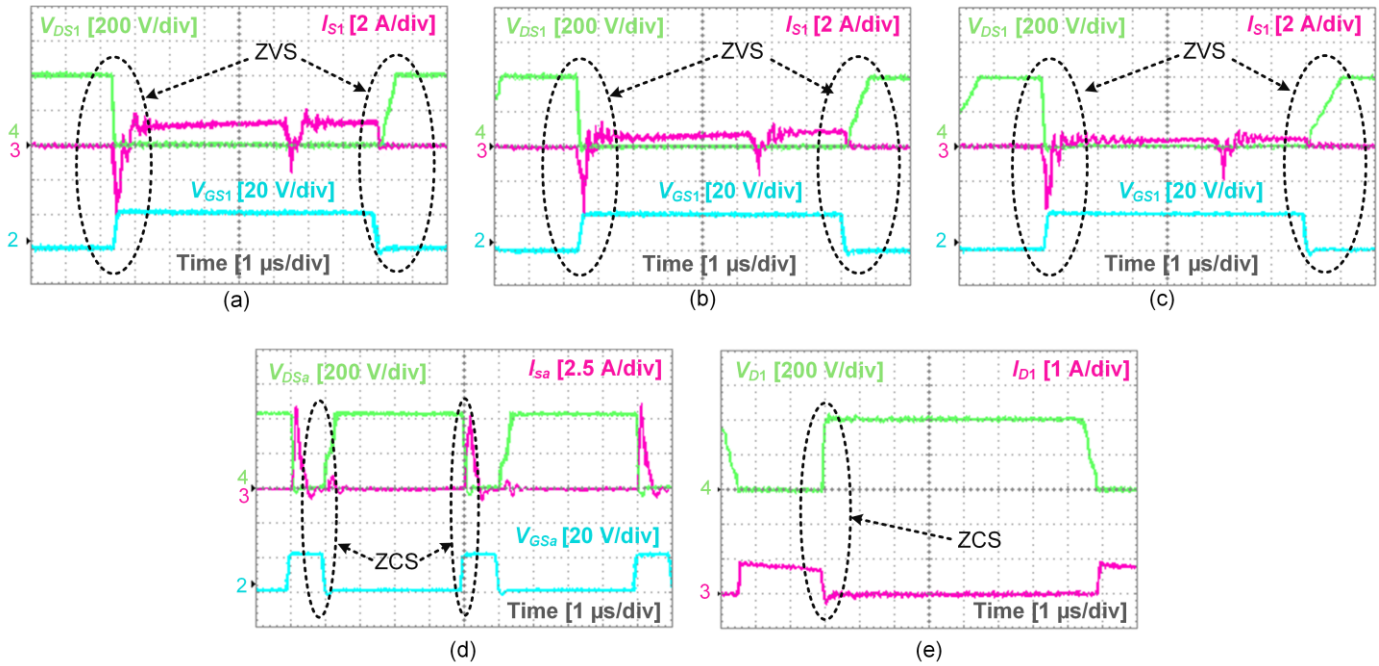

Fig. 5. Experimental voltage and current waveforms. (a) S_1 at full load. (b) S_1 at half load. (c) S_1 at 25% load. (d) S_a at full load. (e) D_1 at full load.

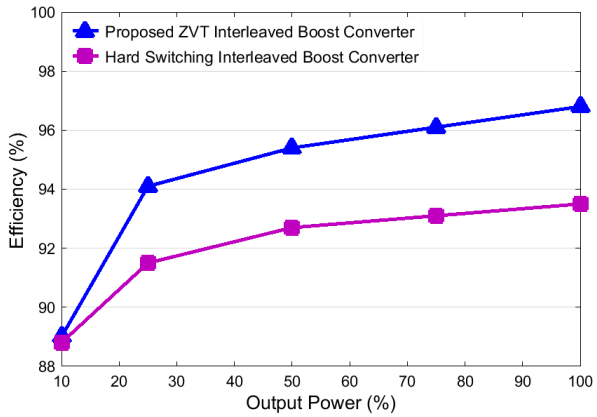

Fig. 6. Efficiency comparison between the proposed ZVT interleaved boost converter and the conventional hard switching counterpart.

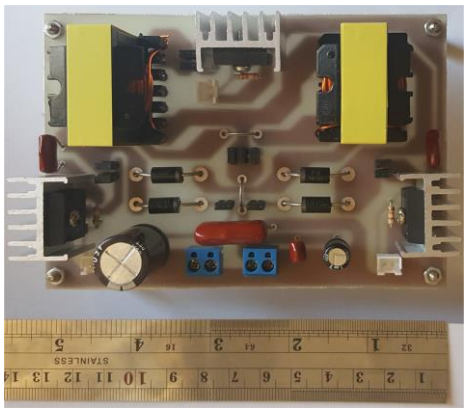

Fig. 7. Photograph of the implemented prototype.

multivibrators, pulse delay units, and logic OR gate are employed to produce the essential gate pulses of the main and auxiliary switches as shown in Fig. 4(b).

Fig. 5(a) to 5(c) show the experimental voltage and current waveforms of the main switch S_1, at nominal load, half load, and 25% of nominal load conditions, respectively. This figures clearly illustrates how the main switch turns on and off under ZVS condition even at light load. Besides, as can be observed from this figure, the voltage and current stresses of the main switch are like the ones in conventional hard switching interleaved boost converter and hence, no extra voltage and current stresses are imposed on the main switch. Fig 5(d) shows the voltage and current waveforms of the auxiliary switch, S_a at nominal load. From this figure, ZCS turn on and turn off of S_a can be seen. Fig. 5(e) shows the voltage and current waveforms of the output diode D_1 at nominal load. As this figure shows, D_1 achieves ZCS at turn off and therefore its reverse recovery problem is alleviated.

A loss breakdown for the proposed ZVT interleaved boost converter and its hard switching counterpart for operating point of V_{in}=100 V is provided in Table II. All other converter parameters are the same as the design example. As observed, the auxiliary elements contribute an additional loss of about 1.81 W at 200 W nominal output power, while eliminate about 8.94 W switching, snubber and capacitive turn on losses. This signifies a reduction in the total losses from 13.4 W to 6.61 W. Fig. 6 exhibits the efficiency improvement of the proposed ZVT interleaved boost converter as compared to the conventional hard switching counterpart for various output powers. The proposed converter full load efficiency is about 96.8 % which is much higher than that of a conventional hard switching interleaved boost converter.

The features of the proposed converter and the converters presented in [15], [16], [19], [20], and [22] are compared and shown in Table III. As this table indicates, the proposed converter number of elements is equal to that of [15] while the auxiliary switches in the converter of [15] must be unidirectional. The control circuit of the proposed converter is

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TABLE II
COMPARISON OF LOSSES IN THE PROPOSED CONVERTER AND HARD SWITCHING INTERLEAVED BOOST CONVERTER

		Proposed converter	Conventional hard switching converter
Switches $V_{DS(max)}$, $I_{(RMS)}$	S_1, S_2	400 V, 0.89 A	400 V, 0.99 A
	S_a	460 V, 1.09 A	N.A
Diodes V_F, $I_{(ave)}$	D_1, D_2	0.7 V, 0.25 A	0.7 V, 0.25 A
	D_{a1}, D_{a2}	0.7 V, 0.14 A	N.A
Semiconductor devices losses (W)	S_a capacitive turn on loss	1.16	N.A
	S_a switching loss	0	N.A
	S_a conduction loss	0.21	N.A
	D_{a1}, D_{a2} conduction loss	2×0.09	N.A
	S_1, S_2 capacitive turn on loss	0	2×0.44
	S_1, S_2 switching loss	0	2×1.15
	S_1, S_2 conduction loss	2×0.17	2×0.14
	S_1, S_2 snubber loss	0	2×2.88
	D_1, D_2 conduction loss	2×0.17	2×0.17
Core loss (W)		2×0.48	2×0.48
Copper loss (W)		2×0.56	2×0.46
Total theoretical loss (W)		4.3	11.4
Total experimental loss (W)		6.61	13.4

simple, mostly because it has only one auxiliary switch and the source of all the switches, and the converter input and output are common grounded, therefore does not need floating gate driver circuits. Fig. 7 shows the prototype photograph.

VI. OTHER PROPOSED ZVT INTERLEAVED CONVERTERS

Fig. 8 shows proposed two-phase ZVT interleaved buck and buck-boost converters. The related operation principles, design procedure and soft switching considerations of these converters are similar to those explained for the boost type in the previous sections. The number of phases in the illustrated interleaved converters can be increased while using only one auxiliary circuit as long as the transient times to deplete the snubber capacitor and provide ZVS condition at turn on for the main switch does not limit the required converter duty cycle. However, the maximum number of phases is constrained mainly by switching frequency and consequently by parasitic elements.

In the ZVT interleaved buck converter shown in Fig. 8 (a), the source of all MOSFETs are connected to the input ground. Hence, the switches can be derived easily without requiring floating gate driver circuits. However, the input and output grounds of this converter are not common which limits the converter applications. To apply the proposed ZVT cell to common input-output ground interleaved buck converter, the ZVT cell is modified as shown in Fig. 8 (b). The operation of this converter is similar to the converter shown in Fig. 8 (a). In this converter, when D<0.5, before the turn on of each main switch, the auxiliary switch is turned on and the currents of diodes D_1 and D_2 decrease in linear manner until these diodes turn off. Then, the snubber capacitors are discharged through a resonance with the leakage inductance of the coupled inductors and S_1 and S_2 anti-parallel diodes turn on.

VII. VARIANTS OF THE PROPOSED CONVERTERS

In order to make the proposed ZVT interleaved converters topologies more compact and to further reduce the cost, all magnetic elements are coupled together on a single core as shown in Fig. 9. In these proposed topologies, automatic current sharing is established between the interleaved modules and the voltage gain is improved. In addition, no complexity is added to the converter operation. The only drawback of this topology is that the peak current of the main switches is twice the previous version, even though, the average current remains the same. In comparison to the interleaved boost converter presented in [17], the boost type of these proposed family has no auxiliary magnetic core but requires two auxiliary diodes. However, unlike the converter presented in [17] in which the main and auxiliary switches turn off under hard switching condition, the proposed converter is fully soft switched. Besides, in the converter presented in [17], the auxiliary switch is kept ON long enough so that the stored energy in the auxiliary inductor is totally wasted in the circuit.

The operation principles of the new proposed converters are similar to their counterparts presented in Figs. 1 and 8. For instance, the operation of the new boost type (Fig. 9(a)) is briefly explained in the following. Before t_0, it is assumed that all switches are OFF and D_1 and D_2 are ON and transferring energy to the output. Before turning on one of the main switches, for example S_1, S_a turns on and I_{Lka} increases and conversely I_{D1} and I_{D2} decrease linearly until the output diodes turn off. A resonance begins between the snubber capacitors C_{S1} and C_{S2} and L_{Ka} and the snubber capacitors are discharged completely and S_1 and S_2 antiparallel diodes turn on. Therefore, S_1 can be turned on at ZVS. I_{Lka} begins to decrease linearly because of the negative voltage induced by the coupled inductors on L_{Ka} until it reaches zero and S_a is turned off at ZCS. When S_1 turns off, both snubber capacitors begin to charge linearly until their voltages reach V_{out} and D_1 and D_2 turn on.

VIII. CONCLUSION

A family of compact and low-cost interleaved DC/DC converters with zero voltage transition function is presented in this paper. The proposed auxiliary cell provides soft switching for all semiconductor devices by using only one switch and no extra inductor. The ZVT cell provides ZVS at turn on and

TABLE III
FEATURE OF THE PROPOSED INTERLEAVED BOOST CONVERTER COMPARED TO THE MOST PROMINENT ZVT INTERLEAVED BOOST CONVERTERS

Feature	Soft switching	Auxiliary switches count	Auxiliary diodes count	Auxiliary magnetic cores count	Basic control circuit complexity	Floating gate drivers count
[15]	all devices	2 unidirectional	0	1	low	2
[16]	main devices	1	3	1	high	0
[19]	all devices	1	4	2	moderate	0
[20]	all devices	1	3	2	moderate	0
[22]	all devices	1	2	1	moderate	1
Proposed converter	all devices	1	2	0	moderate	0

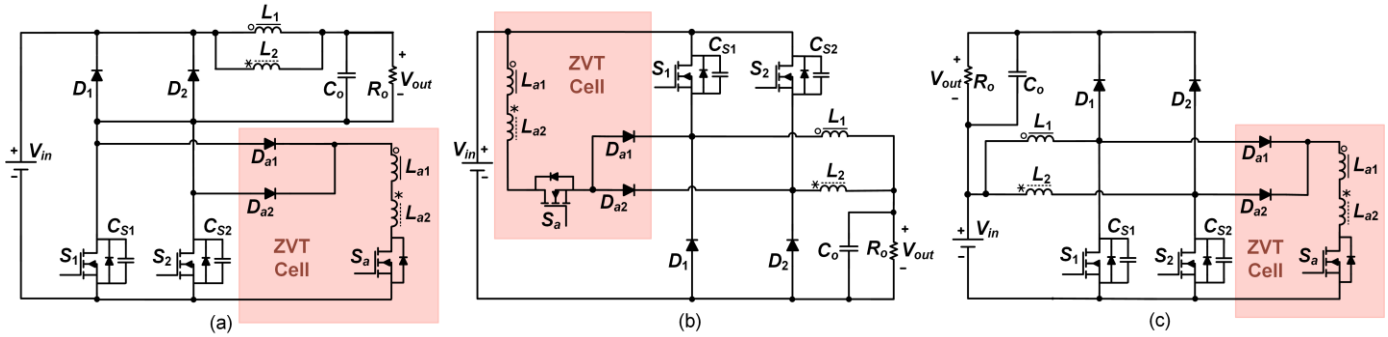

Fig. 8. Different proposed ZVT interleaved converters. (a) ZVT interleaved buck converter. (b) ZVT interleaved buck converter with modified auxiliary cell. (c) ZVT interleaved buck-boost converter.

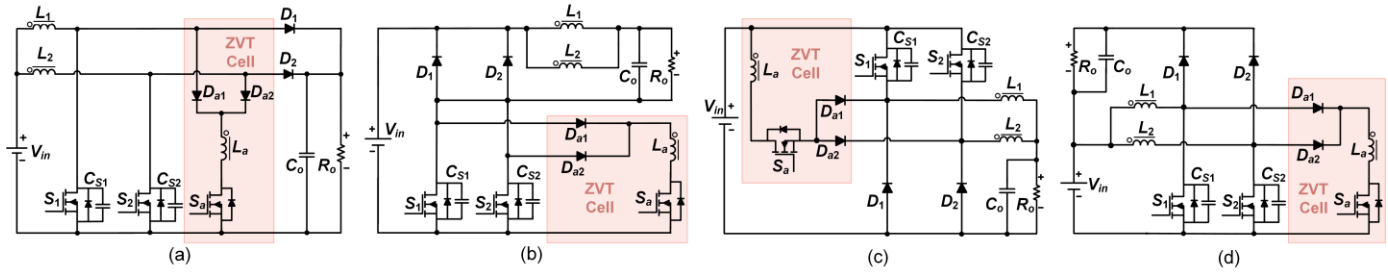

Fig. 9. Variants of the proposed ZVT interleaved converters. (a) ZVT interleaved boost converter. (b) ZVT interleaved buck converter. (c) ZVT interleaved buck converter with modified auxiliary cell. (d) ZVT interleaved buck-boost converter.

ZVS at turn off for the main switches, while the auxiliary switch is turned on under ZCS and turned off under ZVZCS conditions. By turning off the converter diodes at ZCS, the reverse recovery problem is alleviated. Therefore, the switching losses are considerably reduced in the proposed converters. The ZVT cell does not impose any extra voltage and current stress on the interleaved converter devices. The auxiliary circuit absorbs and utilizes the circuit parasitic elements as resonant elements. The theoretical analysis is validated by a prototype of the boost type of the proposed ZVT interleaved converters family operating at 200 W and 100 kHz.

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Baharak Akhlaghi (S'17) was born in Kermanshah, Iran, in 1983. She received the B.S. and M.S. degrees in electrical engineering from Faculty of Engineering, Razi University, Kermanshah, Iran, in 2005 and 2009, respectively, where she was working on applications of artificial neural networks in electrical engineering. She is currently working toward the Ph.D. degree in electrical engineering at the Department of Electrical and Computer Engineering, Isfahan University of Technology (IUT), Isfahan, Iran.

Her current research interests include switching power converters, renewable energies, soft switching high step-up DC/DC converters, and soft switching interleaved DC/DC converters.

Hosein Farzanehfard (M'08) was born in Isfahan, Iran, in 1961. He received the B.S. and M.S. degrees in electrical engineering from the University of Missouri, Columbia, MO, USA, in 1983 and 1985, respectively, and the Ph.D. degree from Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, in 1992.

Since 1993, he has been a faculty member in the Department of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan, Iran. He is the author or coauthor of more than 150 technical papers published in journals and conference proceedings.

His current research interests include high-frequency soft-switching converters, power factor correction, bidirectional converters, active power filters, high-frequency electronic ballasts, and pulse power applications.